Low Voltage GaAs Power Amplifiers for Personal Communications at 1.9GHz

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ABSTRACT:

Personal communication systems operating at 1.9 GHz require high efficiency power amplifiers (PAs) operating at 3V or below. This paper summarizes the results of GaAs PAs constructed in a module and an MMIC format. These PAs operate at 3V with 30dB gain, 28dBm output power and 50% efficiency.

INTRODUCTION:

As more spectrum allocations for personal communications and wireless data between 1.8 and 2.4GHz open up, the need arises for high efficiency power amplifiers (PAs) operating at low voltage. Since portable systems are battery driven the need for better system efficiency is required. As the voltage is lowered, less battery cells are required (less weight), and the power consumption for digital circuitry is reduced. As the industry goes for lower supply voltage the efficiency specifications for the PAs cannot be compromised. This makes high efficiency PA designs more challenging since the voltage swing lost due to the knee voltage becomes more significant. This paper describes the work done to achieve high efficiency 1.9 GHz PAs operating at 3V.

MODULE DESIGN:

The design approach was in two phases, (1) a module using discrete GaAs devices was designed and used to understand the radio application, (2) an fully integrated power amplifier was designed to reduce the size, weight, and cost of the PA.

The module version used depletion mode GaAs MESFET devices with a gate length of 1.2um. These discrete FETs were fabricated in Motorola's CS-1 using the MAFET (Motorola Advanced FET) [1] process. In order to achieve the 30 dB gain required, 3-stages of amplification were required. In order to maximize the efficiency of the module three different device sizes were used with gate widths of 0.5mm, 2.1mm and 12mm A schematic of the module design is shown in Figure 1. To keep the efficiency as high as possible, a negative voltage was required to bias the gates. The gates of the first two stages are tied together, and the third stage is biased separately. This arrangement allows the first stages to be biased near class A, while the third stage is biased as class AB. Separate gate bias also provides versatility to perform gain adjustment and possibly pulse shaping. ON/OFF control of the IPA may be performed by either controlling the gate voltages to pinch-off the FETs or controlling the drain supply voltage.

The design made use of measured small signal scattering parameter data for all the devices operating at the quiescent bias point. A special BeO coplanar fixture was employed to avoid overheating the components (especially the 12mm FET). Large signal models were not available at the time. Thus load pull measurement for the output stage were used to identify the impedance of the output device under large signal conditions. This was done by mounting the 12mm device in a hybrid test fixture and tuning the output load-line with a commercially available slide screw tuner. The load line was tuned such that power, gain and efficiency were optimized. The matching networks were optimized using commercially available linear simulators to obtain the desired performance under both small signal and large signal conditions.

The matching and bias circuitry on the module made use of microstrip transmission lines for inductors and surface mount chip capacitors and resistors. The layout of the module is shown in Figure 2. The total module measures 12 X 23 X 1.75 mm. The printed circuit board was of the single layer Teflon-glass type with ground on the back side to sustain a microstrip transmission mode. Plated through vias were used to provide ground from the front to the back side of the board. The discrete devices were mounted on

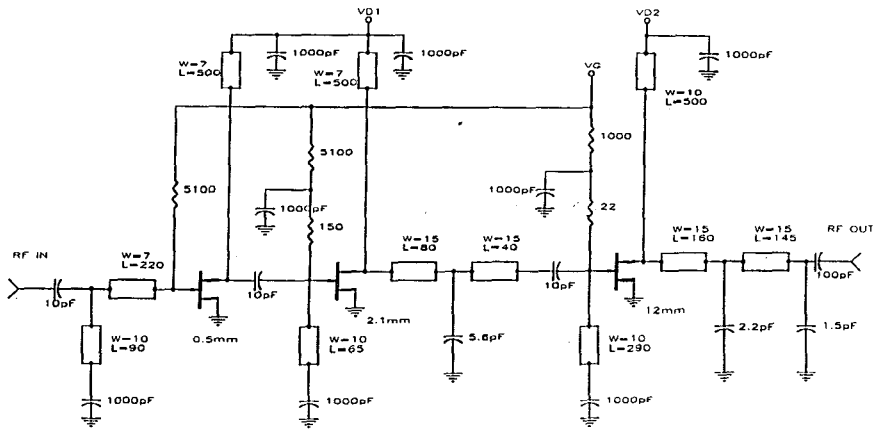

Figure 1 Schematic for the surface mount module.

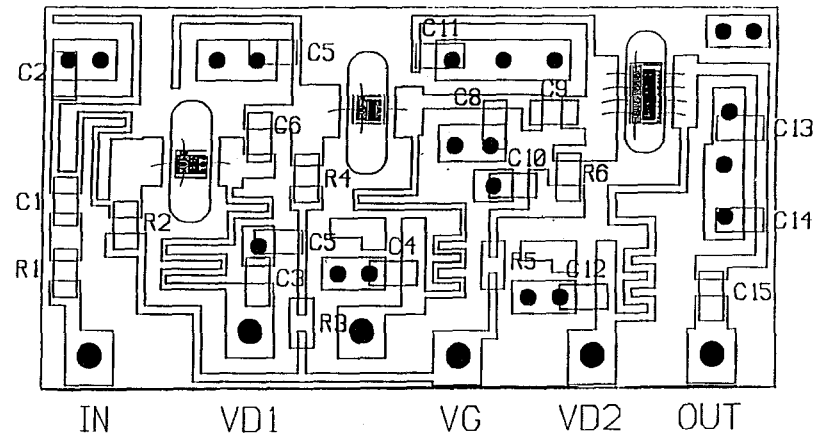

Figure 2 Layout for the surface mount module. (12mmX23mmX1.75mm)

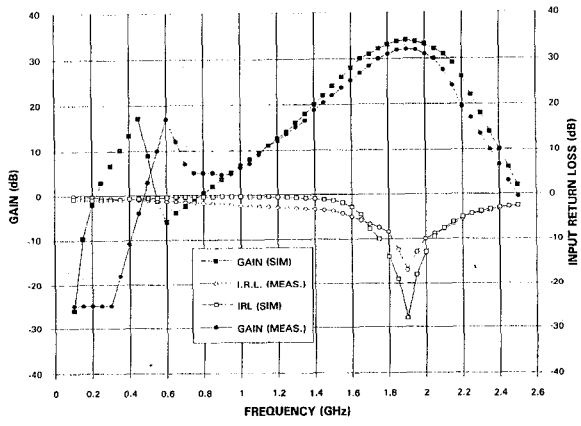

Figure 3. Small signal data, measured vs modeled data for the surface mount module.

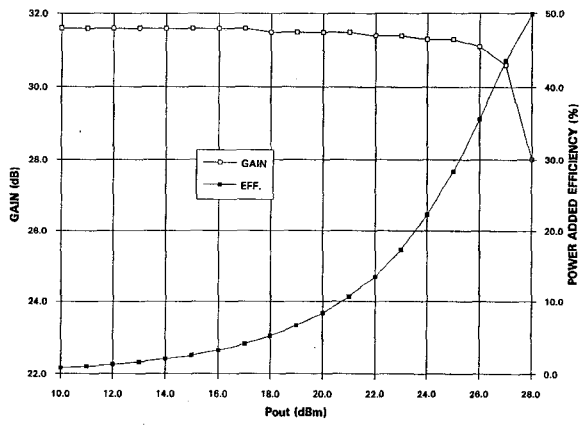

Figure 4. Gain and efficiency vs output power data for the surface mount module.

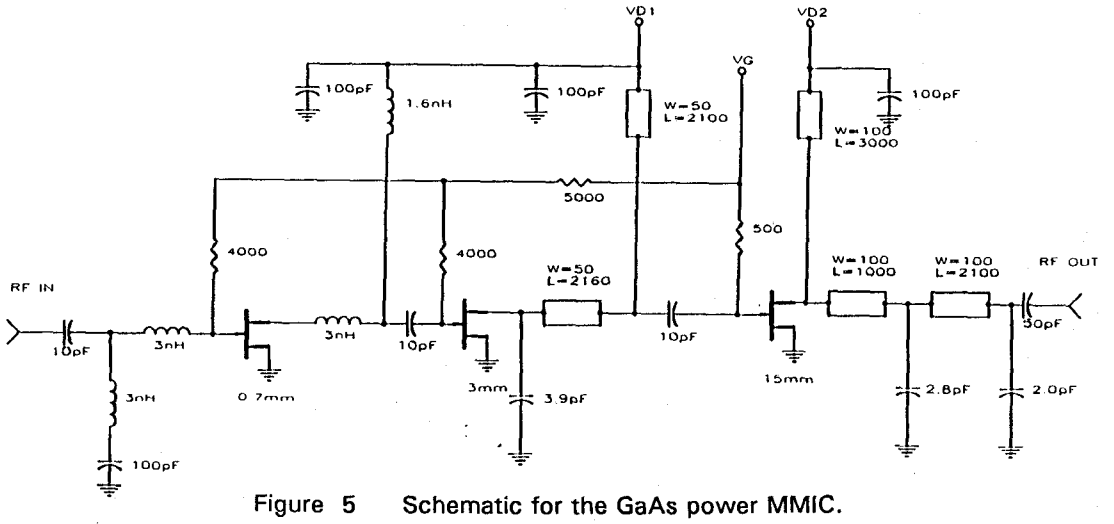

Figure 5 Schematic for the GaAs power MMIC.

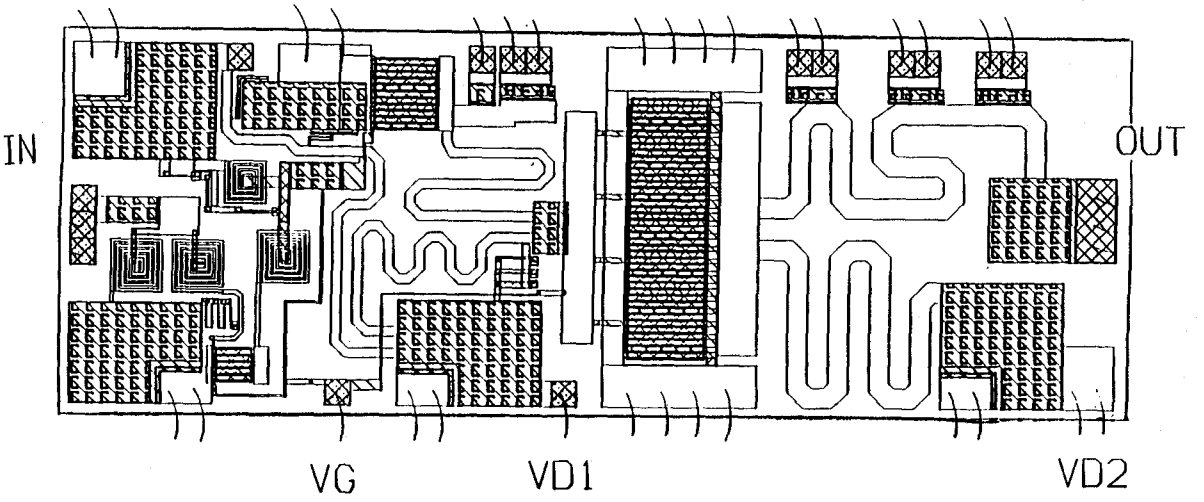

Figure 6 Layout for the GaAs power MMIC. (2mmX2.25mmX.35mm)

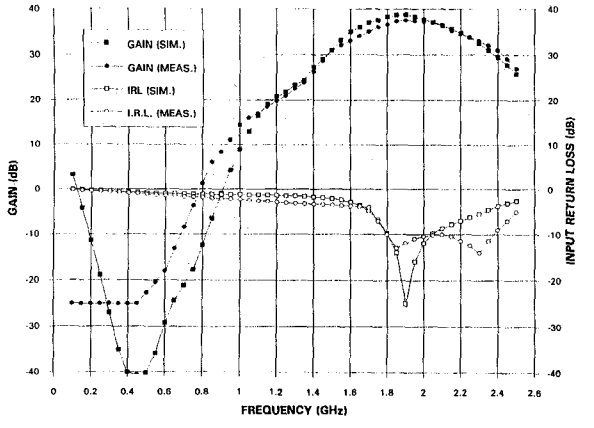

Figure 7. Small signal data, measured vs modeled for the power MMIC.

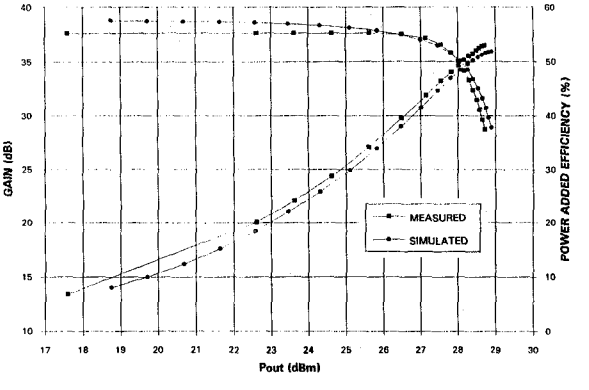

Figure 8. Gain and efficiency data vs output power for the power MMIC.

metal pedestals on the ground plane and placed in holes in the printed circuit such that wire bonding of the devices could be done with ease.

The module produced a small signal gain of 32dB, and input return loss is 17dB. This data is shown in Figure 3 and compares favorably with the simulated data. Under large signal conditions the module had an output power of 28 dBm, and a power added efficiency of 50%. This data is shown in Figure 4.

The system information on the modules was positive and the only marginal spec. was the output power at low battery voltage of 2.7V. In order to insure achieving 28 dBm output power at 2.7V the device sizes for the MMIC lineup were increased.

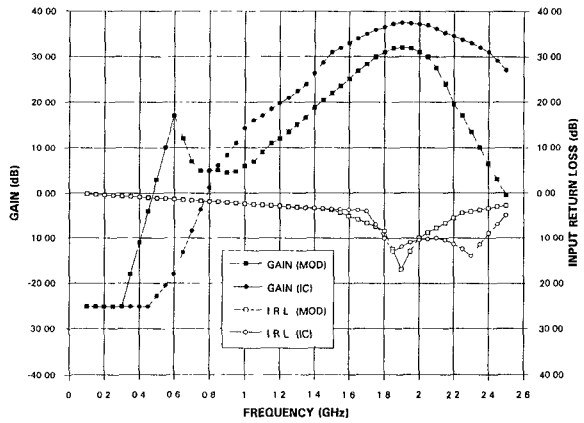

Figure 9. Measured small signal data for the surface mount module vs the MMIC.

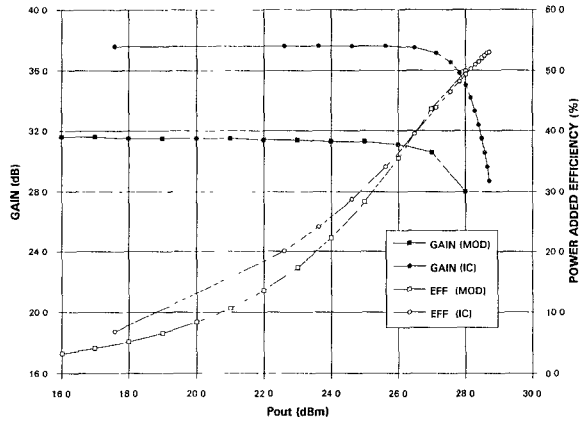

Figure 10. Gain and efficiency vs output power data for the surface mount module vs the power MMIC.

IC DESIGN:

The design methodology for the MMIC was similar to that of the module. The MAFET [1] process used for the MMIC design has a gate length of .8um which provides more gain per stage and thus higher power added efficiency. In order to meet the power specification at 2.7V gate widths were increased to 0.7mm, 3mm and 15mm The circuit topology for the MMIC is similar to the module and is shown in Figure 5. The monolithic design made use of spiral planar inductors, MIM capacitors and bulk resistors on GaAs The layout of the MMIC is shown in Figure 6. The MMIC die size is 2 X 5.25mm. However, with package included, its size is approximately 6.25 X 7.5 mm. Grounding was achieved by using bond wires at the edge of the IC via holes were not used due to the additional cost burden to the process. The source inductance of the 15mm device is critical since excess inductance will consume the gain of the output stage and thus reduce the efficiency. The design required the use of 350 um thick GaAs substrate. This poses a thermal dissipation problem. Thermal simulation of the critical devices was made and the devices were spread out accordingly.

The power MMIC produced a small signal gain of 37dB and an input return loss is 12dB as shown in Figure 7. Under large signal conditions the MMIC has an output power of 28 dBm, an , and a power added efficiency in excess of 50% as shown in Figure 8. The relative measurements of the module vs the MMIC for small signal gain and output power and efficiency are shown in Figures 9 and 10.

CONCLUSIONS:

Results on a surface mount module and an MMIC power amplifier operating at 1.9 GHz and 3V have been demonstrated. Both circuits have demonstrated that GaAs MESFET technology can be used for high efficiency power amplification low voltage for portable communications applications.

ACKNOWLEDGMENT:

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REFERENCE:

[1] B. Cambou. "MMIC Consumer Applications and Production", IEEE Monolithic Microwave and Millimeter-Wave circuits Symp. Dig. p. 1, 1992.